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graph LR; TimeController[Time Controller 110] --> AnalogFrontEnd[Analog Front-end 112]; AnalogFrontEnd -- 114 --> ADA[A/D]; ADA --> Memory[Memory 118]; Memory -- 116 --> DigitalProcessor[Digital (DSP) Processor (μProcessor)];
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The diagram illustrates the system architecture. It features a central horizontal flow of data from left to right. At the top, a 'Time Controller' block (110) is connected to the 'Analog Front-end' block (112) and the 'Digital (DSP) Processor (μProcessor)' block. The 'Analog Front-end' block (112) contains an 'A/D' converter block. Data flows from the 'Analog Front-end' block (112) through the 'A/D' converter (114) to the 'Memory' block (118), and then from the 'Memory' block (118) to the 'Digital (DSP) Processor (μProcessor)' block (116).

Figure 1: Receiver Block Diagram

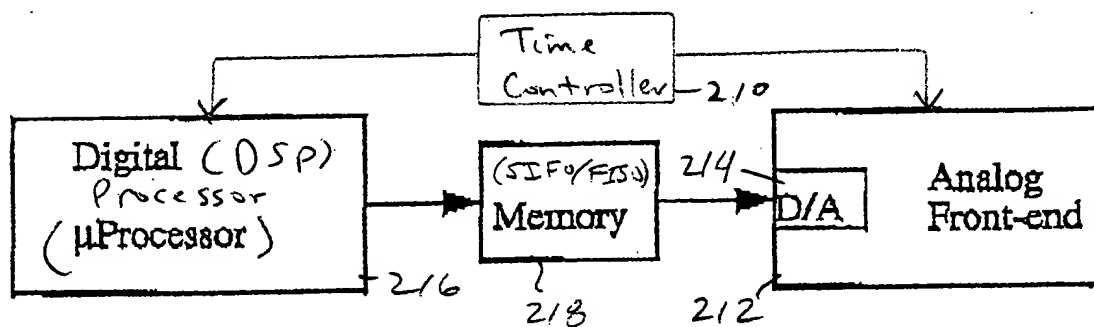


Figure 2: Transmitter Block Diagram

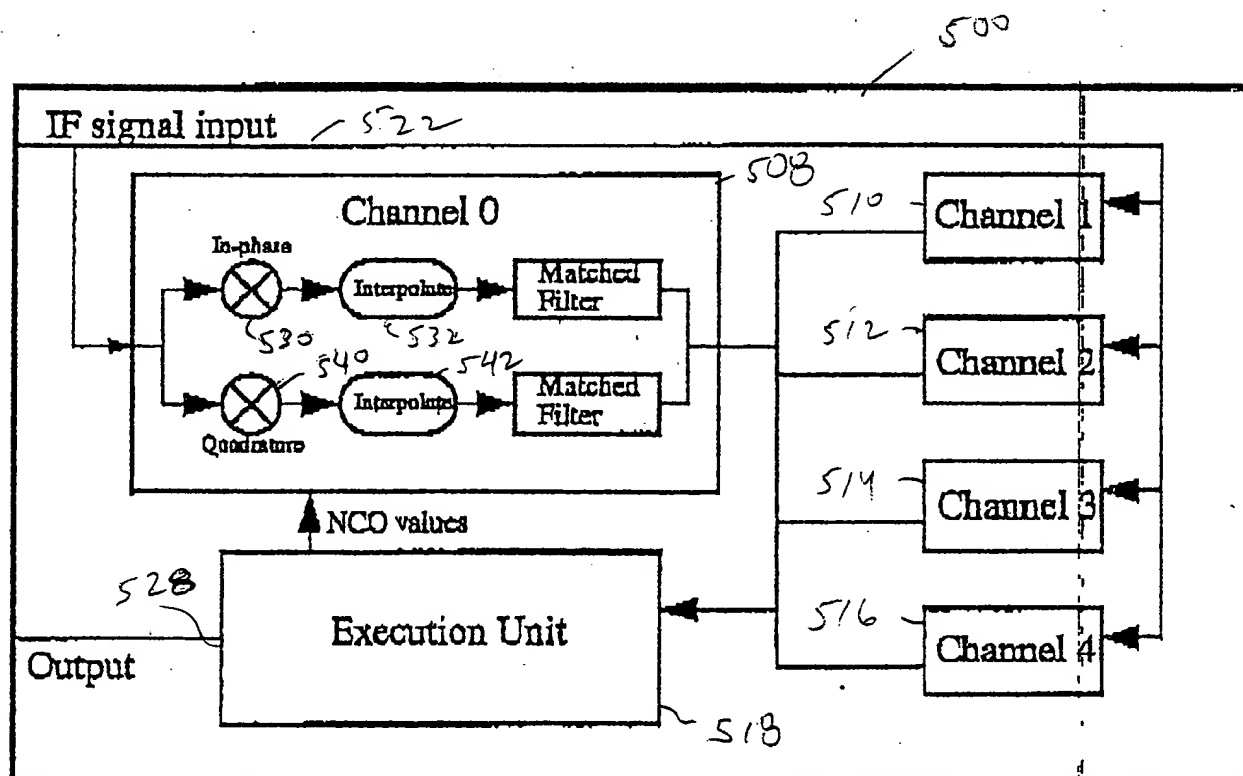


Figure 5 Synchronizer Architecture

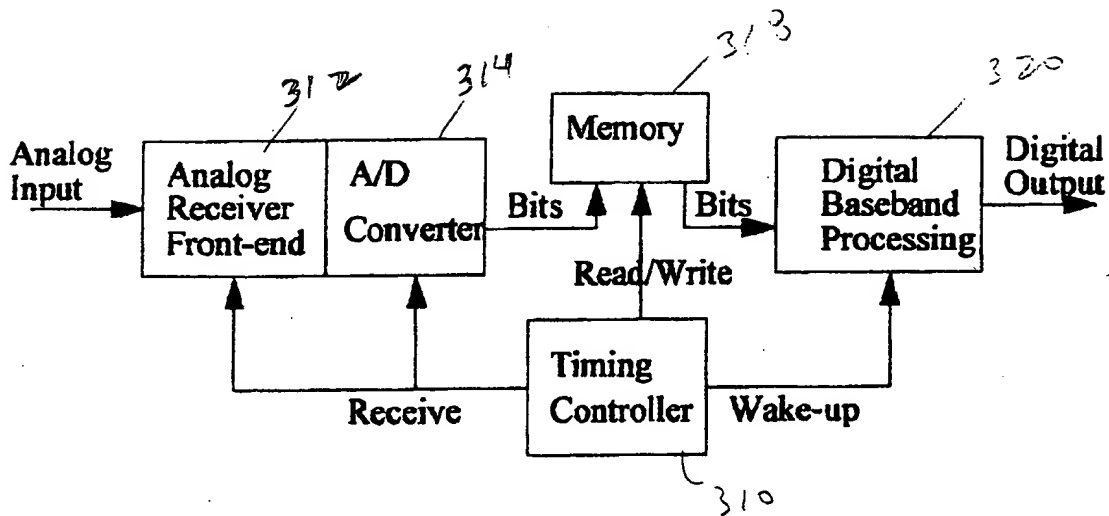


Figure 3 Time-interleaved receiver architecture. The timing controller regulates the receiver operation between the analog receiver front-end circuitry and the baseband processing. It also controls the memory in performing time-interleaving read/write operations.

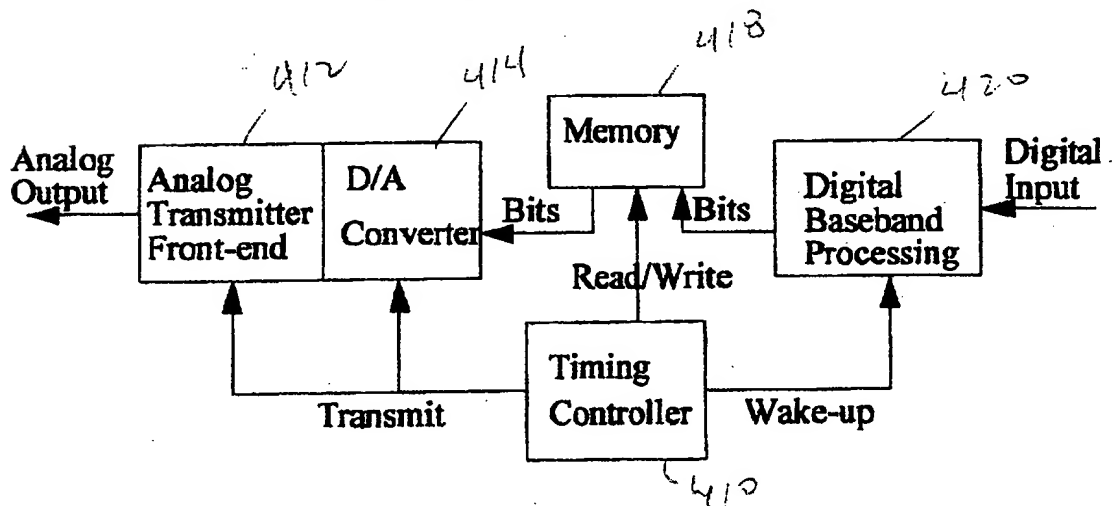


Figure 4. Time-interleaved transmitter architecture. The timing controller regulates the transmitter operation between the analog transmitter front-end circuitry and the baseband processing. It also regulates the memory in performing time-interleaving read/write operations.

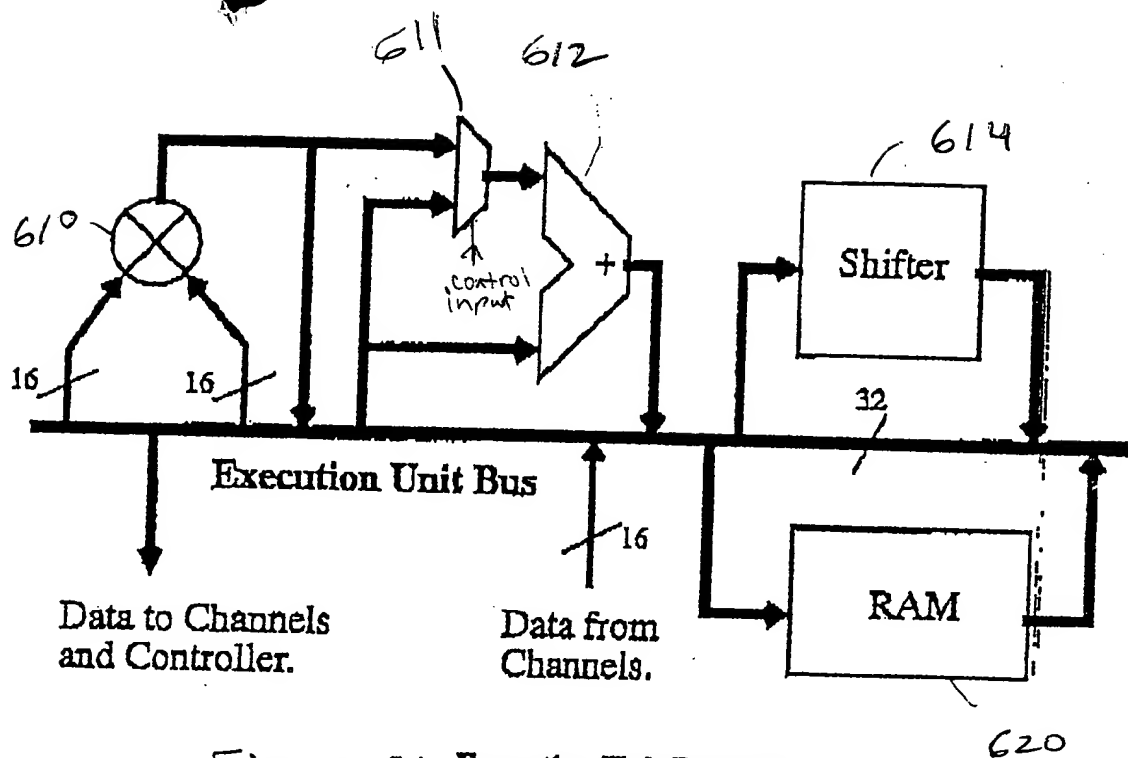


Figure 6: Execution Unit Datapath

